



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/661,328

09/12/2003

Stephen Alan Cohen

YOR920000333US2

9359

7590

10/13/2005

Alvin J. Riddles

P.O. Box 34

New Fairfield, CT 06812-0034

EXAMINER

LE, THAO X

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/661,328

Applicant(s)

COHEN ET AL.

Examiner

Thao X Le

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15 and 17-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15 and 17-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 09/12/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. Figures 1A and 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 17 depends on canceled claim 16.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2814

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5592024 to Aoyama et al in view of US 6245663 to Zhao et al.

Regarding claims 18, Aoyama discloses in a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members 515 pass through a portion of a bulk dielectric 509 substrate 501, col. 25 line 13, and through a mask layer 511 atop said dielectric layer 509 to a common surface, an improvement comprising the intermediate steps of: etching trench and via shape opening out, fig. 31H, of dielectric body 509 through mask layer 510/511 in a region below surface, lining open with thin electrically conductive diffusion barrier layer 514, fig. 31J, electroplating a thick metal 515, column 27 line 4, and filling opening surface planarizing over coated surface through chemical mechanical operation, column 27 line 18, and removing mask layer 511 in all portion between opening to a depth that

Art Unit: 2814

establishes a selected dimension of the upper surface of mask 510 below the surface (upper surface of layer 515), fig. 31L, depositing a protective cap film 516, col. 27 line 24, on exposed surface and remaining exposed surface said cap film 516 minimizing leakage and improving electrical reliability

But, Aoyama does not disclose coating liner layer 514 with a thin metal layer (seed layer).

However, Zhao discloses a method in fig. 4A-4I of making a interconnect structure having plug 420, col. 6 line 10, a barrier layer (TiN), col. 6 line 12, and a seed layer, col. 7 lines 40-45. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the seed layer teaching of Zhao with Aoyama's process, because seeding layer would have helped in delivering electron current uniformly on the wafer for initiation of copper plating as taught by Zhao in col. 8 lines 15-18.

With respect to 'cap film minimizing leakage and improving electrical reliability', Aoyama discloses a structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 15, 19-21, Aoyama discloses the process wherein the mask layer 510 is silicon nitride, column 26 line 40, wherein the diffusion barrier layer 514 is Ti, TiN, column 26 line 61, wherein thick metal 515 comprises copper, column 27 line 2.

Regarding claim 22, Aoyama discloses the process of preventing high electric field concentration in a surface of a dielectric body 509 at a faceted shaped intersection with sub 250 nanometer range size and spacing conductive interconnect members 515 in said dielectric body 509, comprising the steps of depositing a bulk layer of intralevel dielectric material 509 on a silicon substrate 501; etching using a mask layer 510/511, via and trench openings as used in damascene structure, the mask layer 510/511 formed of a material that is hardened relative to the hardness of said dielectric body (509 is silicon oxide or doped with fluorine, column 25 line 15-20, while 510/511 is nitride layer or silicon carbide, column 26 line 40 and col. 25 line 45; thus, the mask layer would be harder than that of inter dielectric layer) which surrounds a conductive layer 515 and which has an upper surface; coating said etched openings with conductive diffusion barrier liners 514 using sputtering method, column 26 line 64, said liner serving as an adhesion barrier between said intralevel dielectric and copper 515, said liner 514 also acting as an electroplating conductor; electroplating and filling said etched openings with additional copper to form copper conductors 515; polishing using chemical or mechanical means so that said copper conductors 515 are nearly coplanar with said upper mask surface; removing said mask layer 511 in all portions between said etched openings to a depth that establishes a selected dimension of the upper surface of said mask 510 below said surface; depositing a protective cap film 516 on exposed

Art Unit: 2814

overcoated surface and remaining exposed surface, said cap film minimizing leakage and improving electrical reliability.

But, Aoyama does not disclose coating liner layer 514 with a thin metal layer (seed layer).

However, Zhao discloses a method in fig. 4A-4I of making a interconnect structure having plug 420, col. 6 line 10, a barrier layer (TiN), col. 6 line 12, and a seed layer, col. 7 lines 40-45. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the seed layer teaching of Zhao with Aoyama's process, because seeding layer would have helped in delivering electron current uniformly on the wafer for initiation of copper plating as taught by Zhao in col. 8 lines 15-18.

With respect to 'cap film minimizing leakage and improving electrical reliability', Aoyama discloses a structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

In the recitation 'the process of preventing high electric field concentration in a surface of a dielectric body at a faceted shaped intersection with sub nanometer range size and spacing conductive interconnect members in said

dielectric body' has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

With respect to 'CVD' vs. 'sputtering' method, Zhao discloses the barrier layer can be deposited by either sputtering or CVD, col. 8 lines 18-22. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the process teaching of Zhao in Aoyama's method, because such process substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

Response to Arguments

7. Applicant's arguments with respect to claims 15,17-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

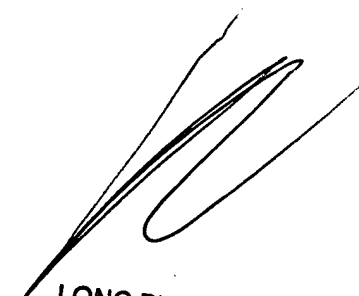
TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
05 Oct. 2004



LONG PHAM
PRIMARY EXAMINER